



[Vivado Xilinx License Crack Software](#)

The screenshot shows the ISE Project Navigator interface with the Design Summary report open. The report is titled 'rolling Project Status' and contains the following data:

Property	Value	Property	Value
Project File:	edf_flow.xise	Parser Errors:	No Errors
Module Name:	countera	Implementation State:	New
Target Device:	xa3s100e-4vqg100	•Errors:	
Product Version:	ISE 12.3	•Warnings:	
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:		•Final Timing Score:	

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report					
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Report Name	Status	Generated
ISIM Simulator Log	Current	Fri Mar 4 13:15:41 2011

Date Generated: 03/05/2011 - 08:58:36

The Errors window at the bottom shows the following messages:

```
ERROR: HDLCompiler:806 - "C:/Documents and Settings/shiva/desktop/vlsi2/hot_rolling.vhd" Line 7: Syntax error near "port".
ERROR: ProjectMgmt:496 - 1 error(s) found while parsing design hierarchy.
```



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